IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Group Art Unit: Unassigned Examiner: Unassigned

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Applicant(s)	:	KUMAMOTO et al.)	
Serial No.	:	Divisional of Appl. Serial No. 09/504,874)	
Filed	:	January 30, 2004)	INFORMATION DISCLOSURE
For	:	SEMICONDUCTOR CHIP AND PRODUCTION PROCESS THEREFOR)	<u>Discheseite</u>
Attorney Ref		AT 318 D1)	L 20

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Sir:

In accordance with the duty of disclosure, attached are copies of the Forms PTO-892 from the parent application, serial number, **09/504,874**, which the Examiner may wish to consult during examination of this Divisional Application thereof.

Respectfully submitted,

January 30, 2004 Date

Steven M. Rabin (Reg. No. 29.102)

RABIN & BERDO, PC Customer No. 23995

Telephone: 202-371-8976 Facsimile: 202-408-0924

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Applicant/Patent
Kumamoto et al

Examiner
Nitin Parekh

Application/Control No.
09/504,874

Art Unit
2811

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¹ Dates in MM-YYYY format are publication dates.

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² Classifications may be U.S. or foreign.

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